REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 4, 2003, and the references cited therewith.

Claims 17 and 23 have been amended, no claims have been added and no claims have been canceled. Thus, claims 1-23 are now pending in this application.

§102 Rejection of the Claims

Claims 1-8, 10, 11, 14-20, 22 and 23 were rejected under 35 USC § 102(e) as being anticipated by Deao et al. (U.S. 6,065,106, hereinafter referred to as Deao). Applicant respectfully traverses this rejection because Deao does not anticipate the claimed invention, as set forth in claims 1-8, 10, 11, 14-20, 22 and 23.

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). Applicant respectfully submits that the Office Action did not make out a *prima facie* case of anticipation because the reference does not teach each and every element of the rejected claims.

In the following discussion of the rejected claims, Applicant will first present a brief summary of Deao. Next, applicant will discuss independent claims 1, 6, 10, 17, 20, and 23 in light of Deao. Last, Applicant will discuss the rejected dependent claims.

Deao will now be summarized. Deao describes a system for debugging and emulating an integrated circuit with an external test system. *See* Abstract of Deao. As shown in Figure 1, the integrated circuit 42 is connected to a test system 51, which is external to the integrated circuit 42. When the system is performing emulation operations, "a sequence of debug instructions is scanned into the multi-word instruction register from external test system 51." Deao col. 51,

lines 62-64. According to Deao, the system is configured so that "a packet of instructions can be transferred from the emulation unit to the instruction register of the processor via a test port and executed ***without fetching instructions from the instruction memory***." (Emphasis Added) Deao at Abstract. The debug instructions are not loaded into memory so as "to prevent extraneous operations from occurring which could otherwise affect memories..." Deao at Abstract.

Claim 1 recites "a memory hierarchy" and "a processor coupled to the memory hierarchy, wherein the processor is configured to test itself by repeatedly executing a plurality of instructions ***using a replay handler loaded into the memory hierarchy***." (Emphasis Added) In contrast, as noted above, Deao describes transferring debug instructions into an instruction register via a test port *without fetching the debug instructions from memory*. Thus, Deao does not teach each and every element of claim 1 because Deao's system does not teach a replay handler loaded into a memory hierarchy.

Claim 6 recites "a processor coupled to the system bus, wherein the processor executes instructions from the memory hierarchy and wherein on a break, the processor reaches a steady state, transfers original code of the memory hierarchy to the storage element, **loads a replay handler into the memory hierarchy** and the processor executes the replay handler to repeatedly replay at least one execution to test for proper operation of the processor, wherein the at least one execution includes a plurality of instructions." (Emphasis Added) Claim 10 recites a "processor to load the replay handler into the memory hierarchy and repeatedly replay the at least one execution." In contrast, Deao describes transferring debug instructions into an instruction register via a test port *without fetching the debug instructions from the instruction memory*. Thus, Deao does not teach each and every element of independent claims 6 and 10 because Deao's system does not teach a replay handler that is loaded into a memory hierarchy.

Amended independent claim 17 recites "loading a replay/restart kernel into a memory hierarchy." As similarly discussed above, Deao does not teach each and every element of amended independent claim 17 because Deao's system does not teach loading a replay/restart handler into a memory hierarchy.

Independent claim 20 recites "loading a replay handler into the instruction cache." As similarly discussed above, Deao does not teach each and every element of amended independent

claim 20 because Deao's system does not teach loading a replay/restart handler into a memory hierarchy.

Independent claim 23 recites "loading a replay handler into a memory hierarchy." As similarly discussed above, Deao does not teach each and every element of amended independent claim 23 because Deao's system does not teach loading a replay/restart handler into a memory hierarchy.

Claims 2-5, 7-9, 11-19, and 21-22 depend, directly or indirectly, on claims 1, 6, 10, 17, and 20, and are patentable over Deao for the reasons argued above, plus the elements in the claims.

§103 Rejection of the Claims

Claims 9, 12, 13 and 21 were rejected under 35 USC § 103(a) as being unpatentable over Deao. Applicant respectfully traverses this rejection because the Office Action has not established a *prima facie* case of obviousness regarding 9, 12, 13 and 21.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one

> of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Dependent claims 9, 12, 13 and 21 include all the limitations of the claims from which they depend. Therefore, each of the rejected dependent claims include limitations for loading a replay handler/replay kernal into a memory hierarchy or cache (see the independent claims for the exact language). As discussed above, Deao describes debugging an integrated circuit *without fetching debug instructions from memory.* However, Deao does not teach or suggest loading a replay handler/replay kernel into a memory hierarchy or cache, as claimed in the rejected dependent claims. Therefore, Deao does not teach or suggest all the limitations of rejected dependent claims 9, 12, 13, and 21.

Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

Conclusion

Based on the foregoing, Applicant respectfully requests that the rejections be withdrawn. Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 371-2169 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KIRAN A. PADWEKAR

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2169

Date 11/04/03

By Andrew DeLizio
Andrew DeLizio
Reg. No. 52,806

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 4th day of November 2003.

Anne M. Richards
Name

Anne M. Richards
Signature